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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Mikio ODA, et al.	**Examiner:**	Unassigned
Serial No:	10/584,735	**Art Unit:**	Unassigned
Filed:	June 26, 2006	**Docket:**	19993
For:	Optical-Element Integrated Semiconductor Integrated Circuit and Fabrication Method Thereof	**Dated:**	November 13, 2006

Mailstop PCT
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

Enclosed is a translation of the International Preliminary Report on Patentability. Please note that the references cited in the International Preliminary Report on Patentability were filed in an Information Disclosure Statement dated June 26, 2006.

Inasmuch as this Information Disclosure Statement is being submitted in accordance with the schedule set out in 37 C.F.R. § 1.97(b), no statement or fee is required.

Respectfully submitted,

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CERTIFICATE OF MAILING UNDER 37 C.F.R. § 1.8(a)

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mailstop PCT, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450.

Dated: November 13, 2006

Thomas Spinelli

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